PATENT ABSTRACTS OF JAPAN

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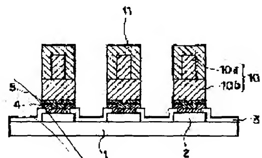
(71)Applicant : OKI ELECTRIC IND CO LTD

(72)Inventor : YAMAI SAWAKO
SHIBUYA HITOSHI

(54) SOLDER BUMP FOR CHIP COMPONENT AND ITS MANUFACTURE

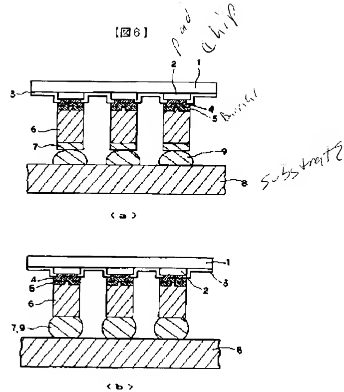
(57)Abstract:

PROBLEM TO BE SOLVED: To provide a solder bump in which the contact area of a first bump with a second bump is made large and in which their exfoliation at the boundary face between both is prevented by a method wherein the second bump is formed in such a way that the surface of a large-diameter pillar-shaped part and the circumferential face and the surface of a small-diameter pillar-shaped part are covered with a solder material whose melting point is lower than that of a solder material for the first bump.



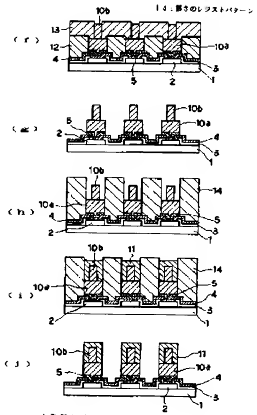
SOLUTION: A diffusion-preventing metal film 5 is formed on a carene film 4 formed on an electrode pad 2 while the carene film is used as an electrode for electrolytic plating. A first bump 10 which is formed in a prescribed height on the diffusion-preventing metal film 5 is composed of a cylindrical large-diameter pillar-shaped part 10b and of a small- diameter pillar-shaped part 10a which is formed on the surface of the large-diameter pillar- shaped part 10b in a diameter which is smaller than that of the large-diameter pillar-shaped part 10b, and both pillar-shaped parts 10a, 10b are formed of the same solder material whose melting point is high. A second bump 11 which is formed in the same diameter as the large- diameter pillar-shaped part 10b so as to cover the surface of the large-diameter pillar-shaped part 10b at the first bump 10 and the circumferential face and the surface of the small- diameter pillar-shaped part 10a is formed of a solder material whose

【図6】



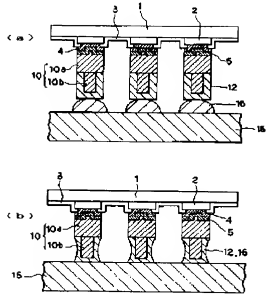
従来例によるチップ部品の実装工程を示す図

【図3】



本発明のバンプ形成工程を示す側断面図

【図4】



実施例によるチップ部品の実装工程を示す図

* NOTICES *

CLAIMS

[Claim(s)]

[Claim 1] The major-diameter pillar-shaped section formed of pewter material on the electrode pad of the chip mounted in a substrate, With the 1st bump who consists of this major-diameter pillar-shaped section and the minor diameter pillar-shaped section formed with the path smaller than this major-diameter pillar-shaped section on this major-diameter pillar-shaped section of the same pewter material, and guarantees the height of the chip to the aforementioned substrate So that the melting point may serve as the same path as the aforementioned major-diameter pillar-shaped section from the pewter material of the 1st bump of the above by low pewter material The pewter bump for chips characterized by consisting of the 2nd bump who fuses by heating and makes connection of the aforementioned chip and the aforementioned substrate in case it is formed so that the peripheral surface and the upper surface of the aforementioned minor diameter pillar-shaped section may be covered from the aforementioned major-diameter pillar-shaped section upper surface, and the aforementioned chip is mounted in the aforementioned substrate.

[Claim 2] The 1st resist pattern which has the hole located on the electrode pad of a chip is used as a plating mask. The 2nd resist pattern which has the hole located on this major-diameter pillar-shaped section with a path smaller than the path of this major-diameter pillar-shaped section after forming the major-diameter pillar-shaped section by plating pewter material on the aforementioned electrode pad is used as a plating mask. The minor diameter pillar-shaped section is formed by plating the same pewter material as pewter material on the major-diameter pillar-shaped section. After constituting the 1st bump who consists of the aforementioned major-diameter pillar-shaped section and the minor diameter pillar-shaped section and removing the resist pattern of the above 1st, and the 2nd resist pattern, So that the peripheral surface and the upper surface of the aforementioned minor diameter pillar-shaped section may be covered from the aforementioned major-diameter pillar-shaped section upper surface by using as a plating mask the 3rd resist pattern which has a hole [higher than the 1st bump of the above and] of the same shape as the major-diameter pillar-shaped section The manufacture method of the pewter bump for chips characterized by forming the 2nd bump by plating the low pewter material of the melting point from the aforementioned pewter material.

[Claim 3] The pewter bump for chips characterized by having used as 95% of lead, and 5% of tin composition of the pewter material which forms the 1st pewter bump in the manufacture method of the pewter bump for chips of a claim 1, and a claim 2, and using as 63% of 37% tin of lead composition of the pewter material which forms the 2nd pewter bump, and its manufacture method.

[Claim 4] The pewter bump for chips characterized by having used as 80% of lead, and 20% of tin composition of the pewter material which forms the 1st pewter bump in the manufacture method of the pewter bump for chips of a claim 1, and a claim 2, and using as 63% of 37% tin of lead composition of the pewter material which forms the 2nd pewter bump, and its manufacture method.

[Translation done.]

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S. Patent Dec. 8, 1998 Sheet 2 of 5 5,847,936

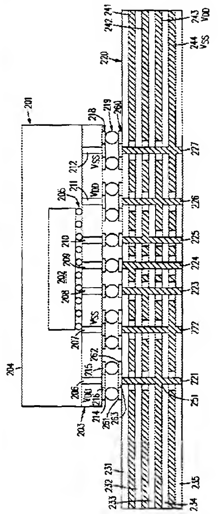

FIG. 3

US-PAT-NO: 5847936

DOCUMENT-IDENTIFIER: US 5847936 A

TITLE: Optimized routing scheme for an integrated circuit/printed circuit board

DATE-ISSUED: December 8, 1998

INVENTOR-INFORMATION:

NAME	STATE	ZIP CODE	CITY	COUNTRY
Forehand; Douglas W.	CA	N/A	Mountain View	N/A
Lamoreaux; Ray	CA	N/A	Milpitas	N/A

ASSIGNEE INFORMATION:

NAME	STATE	ZIP CODE	CITY	COUNTRY	TYPE CODE
Sun Microsystems, Inc.	CA	N/A	Palo Alto	N/A	02

APPL-NO: 08/ 879557

DATE FILED: June 20, 1997

INT-CL: [06] H05K001/14

US-CL-ISSUED: 361/794, 361/748 , 361/751 , 361/762 , 361/760 , 361/764 , 361/765 , 361/777 , 361/807 , 361/808 , 361/820 , 257/700 , 257/738 , 257/774 , 257/778 , 257/773 , 257/787 , 174/250 , 174/255 , 174/256 , 174/260 , 174/261 , 174/265 , 174/266

US-CL-CURRENT: 361/794, 174/250 , 174/255 , 174/256 , 174/260 , 174/261 , 174/265 , 174/266 , 257/700 , 257/738 , 257/773 , 257/774 , 257/778 , 257/787 , 361/748 , 361/751 , 361/760 , 361/762 , 361/764 , 361/765 , 361/777 , 361/807 , 361/808 , 361/820

FIELD-OF-SEARCH: 361/794; 361/748 ; 361/751 ; 361/762 ; 361/760 ; 361/764 ; 361/765 ; 361/777 ; 361/783 ; 361/807 ; 361/808 ; 361/820 ; 257/700 ; 257/701 ; 257/702 ; 257/778 ; 257/737 ; 257/738 ; 257/780 ; 257/773 ; 257/774 ; 257/787 ; 174/250 ; 174/255 ; 174/256 ; 174/257 ; 174/258 ; 174/259 ; 174/260 ; 174/261 ; 174/262 ; 174/265 ; 174/266

REF-CITED:

U.S. PATENT DOCUMENTS

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(28) Isolation layer 601 is a dielectric material, for example, a plating mask or a solder mask. Isolation layer 601 is applied using methods well known in the art such as dry film and etching processes, liquid film and photo-imaging processes, IBM's "SLC" process, or other known fabrication techniques.

(29) Although isolation layer 601 is illustrated in FIGS. 6, 7 and 8, it is understood that step 722 in FIG. 1 is optional and that isolation layer 601 does not have to be formed.

(30) As represented by block 122 of FIG. 1, the metallization 502 (FIG. 6) is formed on substrate bonding contact 501C. Metallization 502 can be a multi-metal-layer metallization. In one embodiment, metallization 502 is formed by applying a copper layer over predetermined portions of substrate bonding contact 501C. Then a nickel layer is selectively applied over the copper layer. Finally a layer of gold or gold alloy is applied over the nickel layer. Generally, the thicknesses of the copper, nickel and gold layers are within the range of 200 micrometers (.mu.m) to 2000 .mu.m, 100 .mu.m to 300 .mu.m and 10 .mu.m to 30 .mu.m, respectively.

(31) In alternative embodiments, metallization 502 is made of, for instance: aluminum; tin over gold over nickel over copper; tin over nickel over copper; lead over gold over tin over aluminum; or tin over lead over gold over tin over aluminum. Metallization 502 is applied using conventional processes such as electroplating or electro-less plating.

(32) As represented in block 131 of FIG. 1, the substrate is next placed into a standard flip chip fixture such as the Flip Chip Aligner/Bonder available from Research Devices in West Piscataway, N.J. as Part No. M8B. The flip chip fixture includes a heater that can be used, as explained below, to heat the substrate during attachment of the chip.

(33) As represented by block 132 of FIG. 1, the chip is held in place above the substrate by the flip chip fixture so that the coined ball bond bumps are aligned above corresponding substrate bonding contacts. The substrate is then heated. The chip is aligned with the substrate using a vision system, as is well known in the art. The chip is picked up with a conventional vacuum tool (not shown). The vacuum tool holding the chip can also include an optional heater which heats the chip.

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ned ball bond the invention. a base section ent of FIG. 4C ations because by application 2 on chip 201 g tool to each e to form the d 4B. , the individu- A and 4B are

preferred due to the pointed shape of the resulting coined ball bond bumps 312.

As represented by block 114 of FIG. 1, integrated circuit chips 201 with coined ball bond bumps 312 are separated by using a conventional sawing process. (In an alternative embodiment, the wafer is first sawn into separate chips 201. The good chips, i.e., electrically and physically sound chips, are then separated from the bad chips. Ball bond bumps 202 are then formed on each of the good chips 201 and each of ball bond bumps 202 are coined, as described above, to create coined ball bond bumps 312.)

As described in detail below, each of the chips 201 are then attached to a substrate by contacting coined ball bond bumps 312 to corresponding metallizations on the substrate bonding contacts.

As represented by block 121 of FIG. 1, a substrate is formed for use with the integrated circuit chip to substrate interconnection according to the invention. The substrate is made of any one of various materials such as organic laminate, ceramic, alumina, silicon, printed circuit board, thin film or flexible circuit. In one embodiment, the substrate is created by a printed circuit board process. The substrate can include one or more layers fabricated and interconnected by methods well known by those skilled in the art.

FIG. 6 is a cross-sectional view of substrate 501 showing upper surface 501A, conductive trace 501B, substrate bonding contact 501C, and metallization 502 in accordance with the present invention.

Conductive trace 501B and substrate bonding contact 501C on upper surface 501A of substrate 501 are typically aluminum and are electrically connected to one another. In one embodiment, conductive trace 501B and substrate bonding contact 501C are formed integrally, for example, are formed from the same layer of conductive material. Conductive trace 501B and substrate bonding contact 501C are created by methods well known in the art. It is to be understood that, on the entire substrate 501, there are a plurality of conductive traces 501B and substrate bonding contacts 501C formed on upper surface 501A.

As represented by block 722 of FIG. 1, optionally, an isolation layer 601 (FIG. 6) can be formed over substrate 501 and conductive trace 501B. As shown in FIG. 6, isolation layer 601 is patterned such that isolation layer 601 leaves uncovered a portion of substrate bonding contact 501C. Isolation layer 601 ensures that metallization 502 is applied only to substrate bonding contacts 501C. Isolation layer 601 is particularly useful when the manufacturer wants to conserve the amount of material used in forming metallization 502, such as when metallization 502 includes gold or a gold alloy.

Isolation layer 601 is a dielectric material, for example, a plating mask or a solder mask. Isolation layer 601 is applied using methods well known in the art such as dry film and etching processes, liquid film and photo-imaging processes, IBM's "SLC" process, or other known fabrication techniques.

Although isolation layer 601 is illustrated in FIGS. 6, 7 and 8, it is understood that step 722 in FIG. 1 is optional and that isolation layer 601 does not have to be formed.

As represented by block 122 of FIG. 1, the metallization 502 (FIG. 6) is formed on substrate bonding contact 501C. Metallization 502 can be a multi-metal-layer metallization. In one embodiment, metallization 502 is formed by applying a copper layer over predetermined portions of substrate bonding contact 501C. Then a nickel layer is selectively applied over the copper layer. Finally a layer of gold or gold

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STANDOFF CONTROLLED INTERCONNECTION

TECHNICAL FIELD

This invention relates to a standoff controlled interconnection for use in a soldering process.

BACKGROUND ART

Electronic components and chips are commonly surface mounted to substrates, such as printed circuit boards, through the use of a solder interconnect or joint. In today's vehicles, this electronic packaging is commonly found in the powertrain, chassis control, and entertainment electronic modules.

Such electronic components may be of the leaded or unleaded (leadless) variety. Examples of the unleaded variety include the Leadless Chip Resistor (LCR), the Leadless Chip Capacitor (LCC), and the Leadless Ceramic Chip Carrier (LCCC). These leadless components are commonly formed of ceramic, such as Al_2O_3, and mounted to a printed circuit board by a solder interconnect. The solder interconnect is generally a solder material formed of 37Pb/63Sn weight percent solder.

In contrast to solder interconnects for leaded components having compliant leads, the mismatch of coefficients of thermal expansion between a leadless component and a printed circuit board is borne by the solder interconnect, resulting in an interconnect having a higher strain/stress range and significant plastic deformation, causing the initiation and propagation of creep-fatigue coupled crack growth. As such, solder interconnects for leadless components in electronic packaging often exhibit low cycle thermal and high strain vibrational fatigue failure under harsh under-hood environments.

The magnitude of the plastic and creep deformation is directly associated with the standoff (height) of the solder interconnect, i.e. the gap between the component and the circuit board. The larger the standoff, the less deformation that occurs thus leading to longer component and assembly lives.

In the past, glass or other types of balls have been utilized in joints between components and substrates. Such arrangements are disclosed in U.S. Pat. No. 5,147,084 issued to Behun et al. and U.S. Pat. No. 5,093,986 issued to Mandai et al. The former discloses a ball grid array pattern which uses a solder ball as a joint between the substrates in conjunction with solder paste for attaching the solder ball to each substrate, while the latter discloses forming electrodes using metal balls and conductive adhesives between two substrates. However, the processes disclosed do not control the standoff height and improve fatigue life of the joint.

Consequently, a need has developed for a method of joining a component to a substrate which controls the standoff of the solder interconnect between the component and the substrate, which results in electronic packaging having improved reliability, cycle life and strength. These improvements are expected to increase sale reduced warranty costs.

BRIEF SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method for joining a component to a substrate which controls the standoff between the substrate and the component.

It is a further object of the present invention to provide a method for joining a component to a substrate having improved reliability and durability.

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It is a still further object of the present invention to provide a method for joining a component to a circuit board through the use of reflow soldering which creates a dendritic structure in the solder interconnect.

In carrying out these and other objects, features and advantages, the present invention provides a method for joining a component to a substrate which applies a base solder portion to at least one of the substrate and component and provides a standoff solder portion in the base solder portion. The standoff solder portion has a higher melting temperature than the base solder portion and a height which substantially corresponds to a desired standoff height between the component and the substrate. The component and substrate are positioned relative to each other on the standoff solder portion. The base solder portion is melted under reflow conditions to form a solder joint between the component and the substrate. This joint substantially encapsulates the standoff solder portion, wherein the reflow conditions create a dendritic structure between the base solder portion and the standoff solder portion.

The above objects and other objects, features and advantages of the present invention are readily apparent from the following detailed description of the best modes for carrying out the invention when taken in connection with the accompanying drawings wherein like reference numerals correspond to like components.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram illustrating a deposit of solder paste onto a substrate according to the present invention;

FIG. 2a is a schematic diagram illustrating the application of solder balls to the solder paste, and an epoxy bead, according to the present invention;

FIG. 2b is a schematic diagram illustrating the top plan view of FIG. 2a according to the present invention;

FIG. 3 is a schematic diagram illustrating the mating of a leadless component to the substrate according to the present invention;

FIG. 4 is a schematic diagram illustrating the results of reflow soldering of the leadless component according to the present invention;

FIG. 5 is a schematic diagram illustrating dendrite formation as a result of reflow soldering according to the present invention; and

FIG. 6 is a schematic diagram illustrating the results of reflow soldering on a leaded component according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

A circuit board assembly at various stages of assembly is illustrated in FIGS. 1-4 and 6. Referring to FIG. 1, a base solder portion, shown as solder paste 12, is stenciled, screen-printed or electro-deposited preferably to printed circuit board (PCB) 14, or its surface 16, by techniques generally known in the art. It is, however, contemplated that the solder paste can be similarly applied to the electronic component (discussed herein), in addition to or in place of substrate 14. Typically, eutectic solder paste 12 has an alloy composition of 63Sn/37Pb weight percent solder and a melting point of 183° C. However, other solder pastes of tin/lead (Sn/Pb) alloy may be used. Another common example is 60Sn/40Pb (the ratios for solder alloys discussed herein are in weight percent solder). The amount of solder

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[11] US005931371A

United States Patent [19]

Pao et al.

[11] Patent Number: 5,931,371

[45] Date of Patent: Aug. 3, 1999

[54] STANDOFF CONTROLLED INTERCONNECTION

[75] Inventors: Yi-Hsin Pao, Livonia; Chao-Jiun Jih, Troy; Jun Ming Hu, Canton; Vivek Amir Jairazbhoy, Farmington Hills; Richard Keith McMillan, II, Dearborn; Xu Song, Westland, all of Mich.

[73] Assignee: Ford Motor Company, Dearborn, Mich.

[21] Appl. No.: 08/784,393

[22] Filed: Jan. 16, 1997

[51] Int. Cl.[6] B23K 31/02; B23K 35/24; B23K 35/14

[52] U.S. Cl. 228/180.22; 228/175; 228/246; 361/770; 361/771

[58] Field of Search .... 228/180.22, 175, 228/245; 361/770, 771; 174/138 D

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Primary Examiner—Samuel M. Heinrich
Assistant Examiner—Jeffrey T. Knapp
Attorney, Agent, or Firm—Richard D. Dixon; Roger L. May

[57] ABSTRACT

A method for joining a component to a substrate applies a base solder portion to the substrate and provides a standoff solder portion in the base solder portion. The standoff solder portion has a higher melting temperature than the base solder portion and a height which substantially corresponds to a desired standoff height between the component and the substrate. The component is positioned on the standoff solder portion and the base solder portion is melted under reflow conditions to form a solder joint between the component and the substrate. This joint substantially encapsulates the standoff solder portion, wherein the reflow conditions create a dendritic structure between the base solder portion and the standoff solder portion.

18 Claims, 2 Drawing Sheets